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(54) Title: MAGNETIC MEMORY
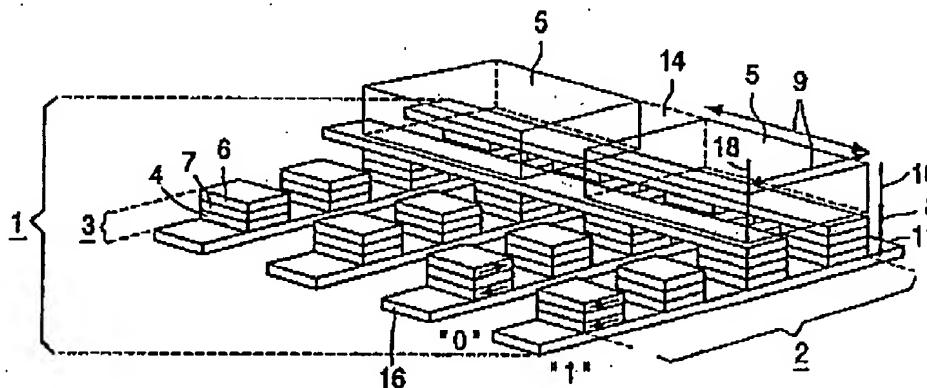
(57) Abstract: The object of the invention is the shielding of a magnetic memory against high external magnetic fields. The magnetic memory (1) comprises an array of magnetic memory elements (2), each memory element (3) including at least one layer of magnetic material (4). The operation of the magnetic memory elements (3) is based on a magnetoresistance effect. The memory (1) is protected against high external magnetic fields by a shielding layer (14), which has been split into regions (5) covering the memory elements (3). The magnetic memory (1) is not erased by high external magnetic fields because of a strong attenuation of the external magnetic field by the regions (5) of the shielding layer (14).

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Magnetic memory

The invention relates to a magnetic memory comprising an array of magnetic memory elements, each memory element including at least one layer of a magnetic material, said memory being provided with a shielding layer against magnetic fields.

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Such a magnetic memory is disclosed in US 5,902,690.

Magnetic memories may take the place of SRAM, DRAM, FLASH and non-volatile memories, such as EPROM and EEPROM owing to the short read and write times, the non-volatile memory and the comparatively low power dissipation. The operation of the

10 magnetic memory elements is based on a magnetoresistance effect, which means that a magnetic field determines the direction of magnetization of the magnetic material, and, when an electric current is sent through the material, the electric resistance depends upon the orientation of the magnetization of the magnetic material. By means of a magnetic field, the direction of magnetization can be switched to two states.

15 One magnetization state corresponds to a comparatively low resistance, a 0, the other state corresponds to a comparatively high resistance, a 1. By directing the magnetization in each memory element by means of a local magnetic field, the memory can be written. External magnetic fields can erase the memory when the magnetic field changes the orientation of the direction of magnetization. Shielding against magnetic disturbing fields

20 is necessary.

In the known memory, the material of the shielding layer is an electrically non-conducting ferrite.

A drawback of the known shielding layer resides in that comparatively strong magnetic disturbing fields of, for example, several tens of kA/m cannot be stopped

25 completely because the ferrite shielding layer becomes magnetically saturated. Once the shielding layer is magnetically saturated, the magnetic field penetrates through the shielding layer, as a result of which the stored magnetization direction in the memory elements can flip over and the non-volatile memory may be erased. Weak magnetic fields of several kA/m are sufficient to erase memory elements.

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In certain applications, for example smart cards, the magnetic memories must be protected against strong magnetic disturbing fields of at least 80 kA/m. Shielding against such strong, external magnetic fields is impossible with the known shielding layer.

Another drawback resides in that the known shielding layer must be thicker as
5 the magnetic disturbing field is stronger. Magnetic memories are often provided on Si semiconductor substrates. In the semiconductor technology, thin-film technologies are employed to apply layers. Shielding layers whose thickness is above 10 μm are very expensive owing to the long deposition time.

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It is an object of the invention to provide a magnetic memory of the type described in the opening paragraph, which is shielded against comparatively strong magnetic disturbing fields of several hundred kA/m.

In the magnetic memory in accordance with the invention, this object is
15 achieved in that the shielding layer is split into mutually separated regions.

A magnetic layer becomes saturated as a result of a magnetic field of sufficient strength. As the shielding layer in the memory in accordance with the invention is split into mutually separated regions, the magnetic field can fan out between the regions. In the magnetic regions of the shielding layer, the magnetic field lines are drawn into the material.
20 The density of the magnetic field lines in these regions is reduced with respect to a continuous layer, as a result of which saturation of the magnetization occurs less rapidly, so that a stronger magnetic field can be shielded than in the case of a continuous shielding layer of the same layer thickness.

Preferably, each memory element comprises, in addition to a first layer of a
25 magnetic material, a second layer of a magnetic material, which is separated from said first layer of magnetic material by a non-magnetic material, because magnetoresistance effects occur in such memory elements which exceed the magnetoresistance effect that occurs in a memory element comprising a single layer of magnetic material.

Spin valves and magnetic tunnel junctions comprise such a layer packet and
30 have the advantage that they can function as a magnetic memory element when the magnetic fields are weak. In its most basic form, a spin valve is a three-layer structure composed of a soft magnetic layer wherein the magnetization changes as a result of a comparatively weak magnetic field, a harder magnetic layer and a noble metal sandwiched therebetween. In a magnetic tunnel junction, the two magnetic layers are separated by an electrical insulation

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layer. As the magnetoresistance effect in spin valves and magnetic tunnel junctions is comparatively large, they can very suitably be used as a magnetic memory element.

The position of the regions of the shielding layer preferably is such that the perpendicular projection of a region on the memory elements comprises at least one memory element. When the dimensions of the memory elements lie in the submicron range, it is advantageous for the perpendicular projection of a region of the shielding layer on the memory elements to comprise a plurality of memory elements, so that the dimensions of the shielding regions can be readily realized and, in general, the shielding effect is also favorably influenced.

In order to provide sufficient shielding against a magnetic disturbing field at the location of the memory elements, two conditions must be met.

First, the magnetization of the material of the shielding layer must remain below the saturation value. Above the saturation value, the field penetrates the material. If the distance between the memory elements and the shielding layer is small, for example 0.5 or less, with respect to the dimensions w of the region, then the magnetization M is given by $M = H_{appl} \chi / (1 + \chi t/w)$, wherein H_{appl} is the external magnetic disturbing field, χ is the magnetic susceptibility and t is the thickness of the shielding layer. The magnetic regions may be of arbitrary shape. In general, the regions will be, for example, rectangular, square, round or hexagonal. The dimensions w of a region then correspond to, respectively, a length and a width, a diameter or a diagonal. Sufficient shielding requires, in the first place, that the following equation is met $t/w > H_{appl}/M_s - 1/\chi$, wherein M_s is the saturation value of the magnetization. If this equation is not met, the shielding layer is subject to saturation.

At this stage, it can be readily understood that, owing to the fact that the shielding layer of thickness t is split into regions, the dimensions w of a region are much smaller than the dimensions w' of a continuous shielding layer extending throughout the surface of the magnetic memory, so that the magnetic disturbing fields can be approximately a factor of w'/w larger before saturation of the magnetization takes place and the magnetic fields are penetrated.

Consequently, as the shielding layer is divided into regions, it is also possible, with a view to shielding against a magnetic disturbing field, to choose the thickness of the shielding layer to be smaller than that of an undivided shielding layer.

Second, it is necessary for the regions of the shielding layer to sufficiently attenuate the magnetic disturbing field, so that the direction of magnetization in the memory elements cannot flip over. Below saturation, the magnetic field at the location of the magnetic

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memory element is given by $H = H_{appl}/(1 + \chi t/w)$. The magnetic disturbing field H_{appl} is attenuated to a much lower magnetic field H at the location of the magnetic memory element, if the following equation is met $t/w > H_{appl}/(H\chi) - 1/\chi$.

Consequently, in order to sufficiently shield each memory element, the
5 following equations must be met $t/w > H_{appl}/M_s - 1/\chi$ and $t/w > H_{appl}/(H\chi) - 1/\chi$. Consequently, it is favorable for the ratio t/w to be as large as possible.

An example: The magnetic disturbing field H_{appl} of 100 kA/m is attenuated to a much lower magnetic field H of 1 kA/m at the location of the magnetic memory element if the following equation is met: $t/w > 100/(1*\chi) - 1/\chi$.
10   Magnetic layers such as FeNi have a comparatively large susceptibility value of, for example, 1000. As a result, the ratio of the thickness of the shielding layer to the dimensions of each region is >0.1:1. It will be clear that the magnetic disturbing field is attenuated less as the t/w ratio is chosen to be smaller. Therefore, it is advantageous if t/w>0.01.

Favorably, the thickness of the shielding layer is much larger than the
15 thickness of the magnetic memory element, for example a factor of 10, so as to ensure that the maximum number of magnetic flux lines of the external magnetic disturbing field pass through the shielding layer, not through the memory elements.

The material of the shielding layer has a magnetic susceptibility which is preferably as large as possible, for example in excess of 100. Preferably, the material also has
20 a high magnetic saturation, for example in excess of 800 kA/m.

The magnetic regions influence the reading and writing of the magnetic memory. For reading and writing a magnetic memory element, a local magnetic field is generated by simultaneously sending a current through a word line and a bit line. The magnetic regions of the shielding layer concentrate the local magnetic field in a magnetic
25 memory element. The word line, through which a comparatively large current is sent, is preferably situated between a region of the shielding layer and a magnetic memory element. As a result, the magnetic material of a region reduces the amount of current necessary for reading and writing a magnetic memory.

Magnetic memories may be integrated with a semiconductor IC. The IC may
30 comprise a silicon substrate with semiconductor devices. Semiconductor devices are, for example, diodes, bipolar transistors or MOS transistors. In general, the magnetic memory is provided on the semiconductor devices. Said semiconductor devices are connected to the magnetic memory by means of metal tracks. The magnetic memory is capable of electrically communicating with an electronic circuit of semiconductor devices in the Si substrate. The

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operation of an electronic circuit may be adversely affected by parasitic capacitances. A continuous shielding layer of an electroconductive magnetic material in combination with the substrate results in a comparatively large parasitic capacitance. Said relatively large capacitance drastically limits the speed of the IC. As the shielding layer is split into regions,

5   the total parasitic capacitance of the shielding layer is substantially reduced, and the operation of the circuit at high frequencies, for example in the GHz range, is improved.

An additional advantage is that the regions of the shielding layer can be arranged over the semiconductor IC in such a manner that semiconductor devices in the IC are shielded against UV light and radiation.

10   If the regions of the shielding layer are situated on top of an IC, said IC is better protected against identification by means of optical methods, owing to the fact that the regions of the shielding layer are not transparent. Besides, the material of the shielding regions is difficult to remove by means of, for example, etching methods, so that reverse engineering of chips is made much more difficult.

15   These and other aspects of the magnetic memory in accordance with the invention will be apparent from and elucidated with reference to the embodiment(s) described hereinafter.

20   In the drawings:

Fig. 1 diagrammatically shows an embodiment of the magnetic memory elements and the regions of the shielding layer;

Fig. 2 shows a magnetic memory element comprising a spin valve and a configuration of a shielding region;

25   Fig. 3 shows an embodiment of a magnetic memory comprising an array of magnetic tunnel junctions.

Fig. 4 is a diagrammatic, cross-sectional view of an embodiment of a magnetic memory integrated with a semiconductor IC.

30

The magnetic memory 1 shown in Fig. 1 comprises an array of memory elements 2. Each memory element 3 comprises at least one layer of magnetic material 4.

In its most basic form, the operation of a memory element 3 is based on an anisotropic magnetoresistance effect (AMR) in a magnetic material.

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An anisotropic magnetoresistance effect (AMR) occurs when the resistance in a magnetic conductor is determined by the angle between the current in the conductor and its magnetization. If the current and the magnetization are oriented in the same direction, then the resistance is highest; if the current and the magnetization extend at right angles to each
5   other, then the resistance is lowest. The difference is typically two to four percent.

A memory element 3 operates better as the magnetoresistance effect is larger.

A giant magnetoresistance (GMR) effect is brought about by spin-dependent scattering in inhomogeneous magnetic systems, such as in a stack of magnetic and non-magnetic metallic layers. If the magnetizations of the individual magnetic layers are switched
10   in one direction by the application of an external magnetic field, then a kind of short-circuit for the electrons with one specific spin direction occurs. As a result, if the magnetizations extend in parallel directions, the resistance is lower than in the case where the magnetizations are anti-parallel. As a result, the resistance in the multilayer may decrease phenomenally to typically approximately 40 to 60% at room temperature. The magnetic field necessary to
15   break the spontaneous magnetic coupling is rather large though, typically several hundred kA/m.

Memory elements which are capable of operating at small magnetic fields are spin-valves and magnetic tunnel junctions. A characteristic feature of these memory elements is that a second layer of magnetic material is separated from the first layer by a non-magnetic
20   material.

A magnetic memory element may alternatively consist of a hybrid of a ferromagnetic and a semiconductor. The magnetic fringing field of the ferromagnet is sufficient to bring about a Hall effect in the semiconductor. The Hall voltage may be positive or negative, i.e. representing a 0 or a 1, respectively.
25   The shielding layer 14 of the magnetic memory is divided into mutually separated regions 5. The regions 5 may be arbitrarily shaped. The shielding regions 5 are preferably situated at the smallest possible distance 8 from the magnetic memory elements 3. A better shielding result is achieved by providing the shielding regions 5 on either side of the memory elements 3. In the embodiment in question, the dimensions of a shielding region 9
30   are such that the perpendicular projection of a magnetic shielding region 5 on the memory elements comprises one memory element 3. If the material of the magnetic shielding regions 5 is a good electrical insulator, as in the case of ferrites, the shielding regions 5 can be provided directly on the memory elements 3. If the material of the shielding regions 5 is electroconductive, preferably, a thin layer of an insulating material of, for example, AlO_x,

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SiO$_2$ or Si$_3$N$_4$ is provided between the magnetic memory elements 3 and the magnetic regions 5. In order to shield the memory elements 3 to the extent possible, the material of the regions 5 preferably exhibits a large susceptibility. A susceptibility value of 1000 can be achieved using, for example, NiFe, CoNbZr, FeSi, FeAlSi.

5   The regions 5 are of a thickness 10, which is generally much larger than the thickness of the magnetic memory element 11, so that the magnetic regions 5 function as a kind of short-circuit for the external magnetic disturbing field.

In Fig. 2, corresponding parts bear the same reference numerals as in Fig. 1. Fig. 2 shows a magnetic memory element 3 comprising a spin valve and a possible
10   configuration of a shielding region 5.

In the embodiment shown, the spin valve 3 is a three-layer structure composed of a first hard magnetic layer 4 of, for example, CoFe, a second, softer magnetic layer 6 of, for example, NiFe which requires only a small magnetic field to change the magnetization, and a non-magnetic metal 7 of, for example, Cu sandwiched therebetween. Each layer is
15   typically 1 to 10 nm thick. The magnetizations of the layers may be oriented so as to be parallel or anti-parallel with respect to each other. In this embodiment, the word line 18 and the bit line 16 serve to write the magnetization direction in the first layer 4 of a selected magnetic memory element 3 and to read the stored magnetization direction from the memory element 3. The word line 18 is situated between a magnetic region 5 and a magnetic memory
20   element 3. Writing takes place by simultaneously sending a comparatively large current through the word line 18 and a current of, for example, 1 mA through the bit line 16, so that the magnetization of the first comparatively hard magnetic layer is directed. Reading of a bit, or in other words the determination of the magnetic orientation of the first layer 4, takes place using a sequence of current pulses having a smaller amplitude which are capable of switching
25   the soft-magnetic layer 6, not the first hard magnetic layer 4. The resistance of the memory element 3 is measured by means of a sense current through the bit line 16 when a sequence of a positive and a negative current pulse is being sent through the word line 18. In this process, the local magnetic field is larger than the switching field of the second, soft-magnetic layer 6 and smaller than the switching field of the hard magnetic layer 4. The first pulse of the pulse
30   sequence places the magnetization of the soft-magnetic layer 6 in a defined starting position. The sign of the resistance change during the second pulse indicates whether the information in the hard-magnetic layer 4 is a 0 or a 1. For a stored 0, the pulse sequence corresponds, for example, to an antiparallel-to-parallel orientation of the magnetization, with the electrical

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resistance changing from high to low. At room temperature, the resistance difference typically is 4 to 18%.

In Fig. 3, corresponding parts bear the same reference numerals as in Fig. 1 and Fig. 2. Fig. 3 shows a possible embodiment of a magnetic memory 1 comprising an array

5 2 of magnetic tunnel junctions 3. In a magnetic tunnel junction 3, two ferromagnetic layers 4, 6 of, for example, CoFe having a thickness of several nanometers, are separated by an insulation layer 7. The insulation layer is 1 to 2 nm thick and is made, for example, from Al_2O_3. By applying a small voltage across the sandwich of magnetic layers comprising the metal oxide 7 between them, the electrons can tunnel through the insulation layer 7. The

10 tunneling probability depends on the magnetic orientation of both magnetic layers 4, 6: the tunneling probability is larger if both magnetic orientations extend parallel to each other. The difference in electric resistance is typically 20-40% at room temperature. In the embodiment shown in Fig. 3, a shielding region 5 extends over four memory elements 3. The distance from the memory elements 3 to the shielding layer 14 is smaller than the dimensions of the

15 region 9. In the magnetic shielding regions 5, saturation of the magnetization caused by the magnetic field must not take place.

Sufficient shielding requires $t/w > H_{appl}/M_s - 1/\chi$ and $t/w > (H_{appl}/H - 1) \chi^{-1}$. At practical values of H_{appl} is 80 kA/m, the saturation value of the magnetization $M_s = 800$ kA/m for NiFe and $\chi = 1000$ and a magnetic field $H = 0.8$ kA/m at the location of the magnetic

20 memory elements 3, a value of $t/w > 0.1$ is achieved.

In Fig. 4, corresponding parts bear the same reference numerals as in Fig. 1, Fig. 2 and Fig. 3. Fig. 4 is a diagrammatic, cross-sectional view of an embodiment of a magnetic memory 1 integrated with a semiconductor IC 12. The Si substrate 13 comprises semiconductor devices, for example diodes, bipolar transistors, MOS devices, or

25 combinations thereof.

The magnetic memory 1 is arranged above the semiconductor devices and connected to said semiconductor devices by metal tracks 15. The semiconductor devices are capable of electronically switching the magnetic memory elements 3. In this embodiment, a MOS transistor 14 is connected to a bit line 16 of the magnetic memory 1. A second MOS

30 transistor 17 selects the word line 18 of the magnetic memory 1. The magnetic memory 1 can be controlled by an electronic circuit manufactured in or on the Si substrate 13.

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CLAIMS:

1.   A magnetic memory (1) comprising an array of magnetic memory elements
(2), each magnetic memory element (3) including at least one layer of a magnetic material
(4), said memory being provided with a shielding layer (14) against magnetic fields,
characterized in that the shielding layer (14) is split into mutual separated regions (5).

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2.   A magnetic memory (1) as claimed in claim 1, characterized in that each
memory element (3) comprises a second layer of a magnetic material (6), which is separated
from the first layer (4) by a non-magnetic material (7).

10 3.   A magnetic memory (1) as claimed in claim 1, characterized in that the
perpendicular projection of a region (5) on the memory elements (2) comprises at least one
memory element (3).

4.   A magnetic memory (1) as claimed in claim 1, characterized in that the
15 memory elements (3) are situated at a distance (8) from the shielding layer (13) which is
smaller than the dimensions (9) of the region (5).

5.   A magnetic memory (1) as claimed in claim 1, characterized in that the ratio
between the thickness (10) of the regions and the dimensions (9) of each region (5) is
20 >0.01:1.

6.   A magnetic memory (1) as claimed in claim 5, characterized in that the ratio
between the thickness (10) of the regions and the dimensions (9) of each region (5) is >0.1:1.

25 7.   A magnetic memory (1) as claimed in claim 1, characterized in that the
thickness (10) of the regions (5) exceeds the thickness (11) of the magnetic memory elements
(3).

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8. A magnetic memory (1) as claimed in claim 1, characterized in that the material of the regions (5) has a magnetic susceptibility above 100.

9. A magnetic memory (1) as claimed in claim 8, characterized in that the
5 material of the regions (5) has a magnetic saturation value above 800 kA/m.

10. A magnetic memory (1) as claimed in claim 2, characterized in that a word line (18) is situated between a region (5) and a memory element (3).

10 11. A magnetic memory (1) as claimed in claim 1, characterized in that the magnetic memory is integrated with a semiconductor IC (12).
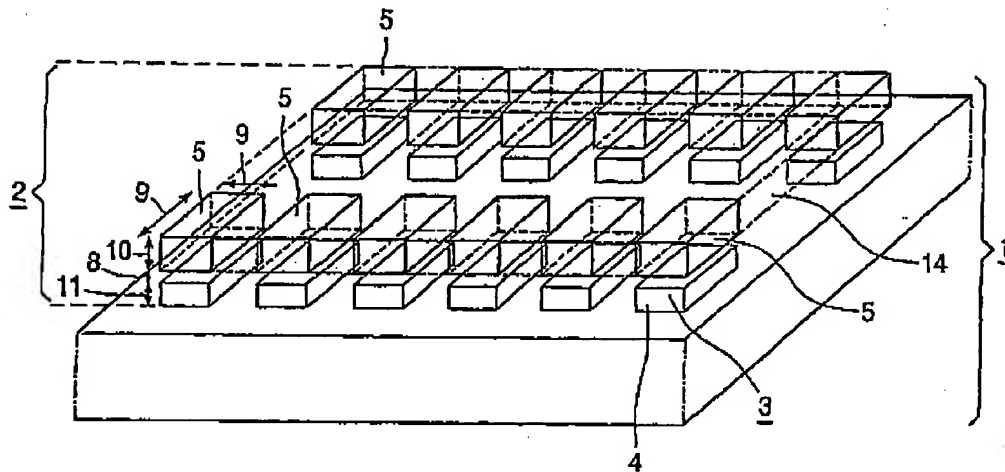
1/2

FIG. 1

FIG. 2

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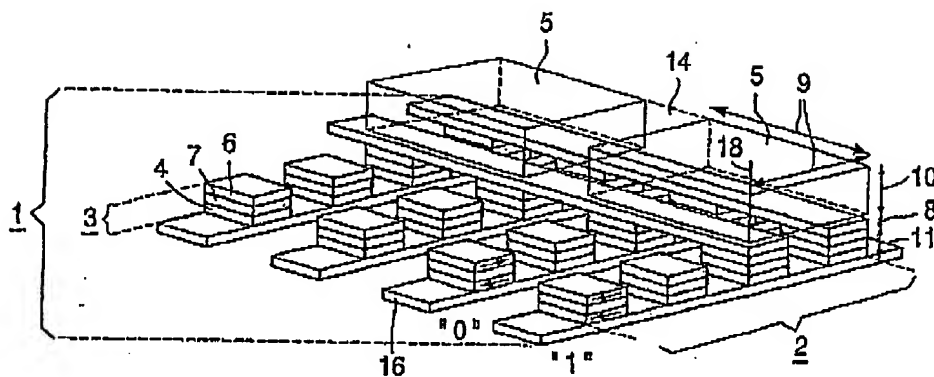
FIG. 3
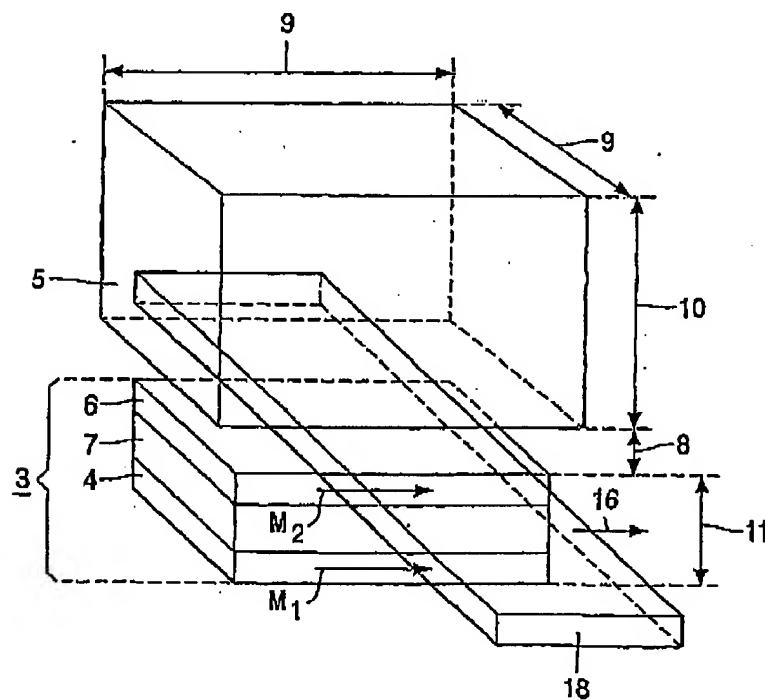

FIG. 4

INTERNATIONAL SEARCH REPORT

onal Application No

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A. CLASSIFICATION OF SUBJECT MATTER

IPC 7   G11C11/16   G11C11/15   G11C11/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7   G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	WO 00 72324 A (HONEYWELL INC) 30 November 2000 (2000-11-30)	1,3,10, 11
A	page 8, line 22 -page 10, line 20 page 15, line 5 - line 15	4-9
Y	US 5 902 690 A (CHEN EUGENE ET AL) 11 May 1999 (1999-05-11)	1-4,10, 11
A	column 4, line 65 -column 5, line 59	5-9
Y	EP 0 776 011 A (MOTOROLA INC) 28 May 1997 (1997-05-28) the whole document	1-4,10, 11

[ ] Further documents are listed in the continuation of box C.   [X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
1 August 2001	08/08/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL — 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Degraeve, L.

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/EP 01/05635

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
WO 0072324	A	30-11-2000	NONE		
US 5902690	A	11-05-1999	DE	19807361 A	27-08-1998
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Form PCT/ISA/210 (patent family annex) (July 1992)